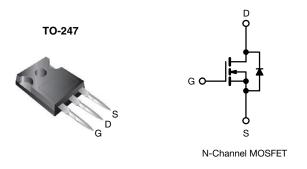
Vishay Siliconix



Power MOSFET



PRODUCT SUMMARY					
V _{DS} (V)	500				
R _{DS(on)} (Ω)	V _{GS} = 10 V	0.40			
Q _g (Max.) (nC)	74				
Q _{gs} (nC)	19				
Q _{gd} (nC)	3	5			
Configuration	Single				

FEATURES

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30 V V_{GS} Rating
- Reduced C_{iss}, C_{oss}, C_{rss}
- Isolated Central Mounting Hole
- Dynamic dV/dt Rated
- Repetitive Avalanche Rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

This new series of low charge Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced Power MOSFET technology the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability of Power MOSFETs offer the designer a new standard in power transistors for switching applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP450LCPbF

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	500	V
Gate-Source Voltage			V _{GS}	± 30	v
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	1_	14	
V_{GS} at 10 V $T_C = 100 ^{\circ}C$			I _D	8.6	A
Pulsed Drain Current ^a			I _{DM}	56	
Linear Derating Factor				1.5	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	760	mJ
Repetitive Avalanche Current ^a			I _{AR}	14	A
Repetitive Avalanche Energy ^a			E _{AR}	19	mJ
Maximum Power Dissipation	T _C =	25 °C	PD	190	W
Peak Diode Recovery dV/dt ^c			dV/dt	3.5	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) for 10 s				300 ^d	
Mounting Torque	6 20 or 1	12 aarow		10	lbf ∙ in
Mounting Torque	6-32 or M3 screw		F	1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = 25 \text{ V}$, starting $T_J = 25 \text{ °C}$, L = 7.0 mH, $R_G = 25 \Omega$, $I_{AS} = 14 \text{ A}$ (see fig. 12). c. $I_{SD} \leq 14 \text{ A}$, $dI/dt \leq 130 \text{ A/}\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150 \text{ °C}$. d. 1.6 mm from case.



www.vishay.com

SHA

IRFP450LC

Vishay Siliconix

Maximum Junction-to-Ambient $P_{In_{JA}}$ - 40 Case-to-Sink, Flat, Greased Surface $P_{In_{JC}}$ 0.24 - 0.65 SPECIFICATIONS T _J = 25 °C, unless otherwise noted Test conditions Min. TVP. MAX. UN Static Drain-Source Breakdown Voltage V _{DS} V _{OS} = 0 V, I ₀ = 250 µÅ 500 - - V Qog Temperature Coefficient $\Delta V_{DS} T_J$ Reference to 25 °C, I ₀ = 1 mÅ - 0.59 - V Gate-Source Threshold Voltage V _{GS} = 0 V, I ₀ = 250 µÅ 2.0 - 4.0 V Zero Gate Voltage Drain Current I _{DS} V _{DS} = 400 V, V _{OS} = 0 V, I _J = 125 °C - - 250 µÅ Orain-Source On-State Resistance P _{DS(M)} V _{DS} = 400 V, V _{OS} = 0 V, I _J = 84 Å ^b - - 0.40 Ω Optamic P V _{DS} = 400 V, V _{OS} = 0 V, I _J = 84 Å ^b - - 2200 - Orain-Source On-State Resistance P _{OS(M)} V _{DS} = 10 V I _D = 84 Å ^b - - 10 0.	THERMAL RESISTANCE RATI	NGS							
Case-to-Sink, Flat, Greased Surface $R_{\rm fb,C}$ 0.24 "C/W Maximum Junction-to-Case (Drain) $R_{\rm fb,C}$ - 0.65 SPECIFICATIONS T _J = 25 °C, unless otherwise noted PARAMETER SYMBOL TEST CONDITIONS MIN. TYP. MAX. UN Optimination of the symbol state Optimination of the symbol state Optimination of the symbol symbol state Optimination of the symbol showing the symbol sym	PARAMETER	SYMBOL	TYP.		MAX.			UNIT	
Waximum Junction-to-Case (Drain) R_{BUC} - 0.65 SPECIFICATIONS T _J = 25 °C, unless otherwise noted PARAMETER SYMBOL TEST CONDITIONS MIN. TYP. MAX. UN Static Drain-Source Breakdown Voltage V_{DS} $V_{OS} = 0$ V, $I_D = 250 \mu A$ 500 - - V Static Vig. Temperature Coefficient $\Delta V_{DS}/T_J$ Reference to 25 °C, $I_D = 1 m A$ - 0.59 - V/V State-Source Threshold Voltage V_{DS}/T_J Reference to 25 °C, $I_D = 1 m A$ - 0.59 - V/V State-Source Threshold Voltage V_{DS}/T_J Reference to 25 °C, $I_D = 100$ - - 4.00 V_V State-Source Chreshold Voltage $V_{DS} = 400$ V, $V_{CS} = 0$ V. - - 2.00 ρ <t< td=""><td>Maximum Junction-to-Ambient</td><td>R_{thJA}</td><td>-</td><td></td><td>40</td><td></td><td></td><td></td><td></td></t<>	Maximum Junction-to-Ambient	R _{thJA}	-		40				
SPECIFICATIONS T _J = 25 °C, unless otherwise noted SPECIFICATIONS T _J = 25 °C, unless otherwise noted State Structure Coefficient SYMBOL TEST CONDITIONS MIN. TYP. MAX UN Structure Coefficient $\Delta V_{DS}/T_J$ Reference to 25 °C, lp = 1 mA - V/P Structure Coefficient $\Delta V_{DS}/T_J$ Reference to 25 °C, lp = 1 mA - V/P Structure Coefficient $\Delta V_{DS}/T_J$ Reference to 25 °C, lp = 1 mA - V/P Structure Coefficient $\Delta V_{DS}/T_J$ Reference to 25 °C, lp = 1 mA - V/P Constance V_DS = 600 V, V_DS = 0 V - 2 P Max V_DS = 500 V, lp = 84 Ab - - 2 P Organ V_DS = 0 V, lp = 14 A, V_DS = 400 V, lp = 14 A, V_DS =	Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.24		-			°C/W	
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Maximum Junction-to-Case (Drain)	R _{thJC}	-		0.65				
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$									
Static Vos V _{GS} = 0 V, I _D = 250 µA 500 - - V Orain-Source Breakdown Voltage $\Delta D_O / J_J$ Reference to 25 $(r, I_D = 1 \text{ mA})$ - 0.59 - V//2 State-Source Threshold Voltage $V_{GS} = W_{GS}$ $V_{CS} = V_{GS}$, $I_D = 250 \mu A$ - 4.0 V//2 State-Source Leakage Ioss $V_{GS} = 420 V$ - - 4.0 V//2 Zero Gate Voltage Drain Current Ioss $V_{GS} = 500 V$, $V_{GS} = 0 V$ - - 250 μ //2 Orain-Source On-State Resistance $R_{DS(m)}$ $V_{GS} = 10 V$ $I_D = 8.4 A^D$ - - 0.40 Ω Optimatic Duptor Capacitance C_{GS} $V_{GS} = 0 V$, $V_{CS} = 25 V$, $f = 1.0 \text{ MHz}$, see fig. 5 - 2200 - - - 320 - - 74 - - 320 - - 74 - - - 320 - - - 74 - - - - - -	SPECIFICATIONS T _J = 25 °C, u	nless otherwi	se noted						
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	PARAMETER	SYMBOL	TEST	CONDIT	IONS	MIN.	TYP.	MAX.	UNIT
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Static								
Sate-Source Threshold Voltage $V_{GS(th)}$ $V_{DS} = V_{GS}$, $I_D = 250 \ \mu$ A 2.0 $ 4.0$ V Sate-Source Leakage I_{GSS} $V_{GS} = \pm 20 \ V$ $ \pm \pm 100$ nA Zero Gate Voltage Drain Current I_{DSS} $V_{CS} = 500 \ V, V_{GS} = 0 \ V, T_J = 125 \ C$ $ 2.50$ μ^{μ} Drain-Source On-State Resistance $R_{DS(on)}$ $V_{GS} = 10 \ V$ $I_D = 8.4 \ A^{D}$ $ 0.40 \ \Omega_{O}$ Ω_{S} Opmanic $V_{DS} = 500 \ V, V_{GS} = 0 \ V, \ V_{DS} = 50 \ V, \ I_D = 8.4 \ A^{D}$ $ 0.40 \ \Omega_{O}$ Ω_{S} Dutput Capacitance C_{ciss} $V_{OS} = 50 \ V, \ I_D = 8.4 \ A^{D}$ $ 2.00 \ 3.20 \ 2.200 \ 2.200 \ 2.200 \ 2.200 \ 2.200 \ 2.200 \ 2.200 \ 2.200 \ 2.200 \ 2.200 \ 2.200 \ 2.200 \ 2.200 \ -$	Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0$	V, I _D = 2	50 μA	500	-	-	V
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, $I_D = 1 \text{ mA}$		-	0.59	-	V/°C	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V	_{GS} , I _D = 2	250 μA	2.0	-	4.0	V
Zero Gate Voltage Drain Current I <	Gate-Source Leakage	I _{GSS}	V _G	_S = ± 20	V	-	-	± 100	nA
Vos 400 V, Vos 0 V, Vos 0 V, Vos - - 250 Drain-Source On-State Resistance R _{DS(on)} V _{GS} = 10 V I _D = 8.4 A ^b - - 0.40 Ω Forward Transconductance grs V _{DS} = 50 V, I _D = 8.4 A ^b 8.7 - - S Dynamic nput Capacitance C _{IBS} V _{OS} = 0 V, V _{OS} = 25 V, f = 1.0 MHz, see fig. 5 - 2200 - Reverse Transfer Capacitance C _{rss} V _{OS} = 25 V, f = 1.0 MHz, see fig. 5 - 28 - Total Gate Charge Qg V _{OS} = 10 V I _D = 14 A, V _{DS} = 400 V, see fig. 6 and 13 ^b - - 19 nc Gate-Source Charge Qgd V _{OS} = 10 V I _D = 14 A, V _{DS} = 400 V, see fig. 6 and 13 ^b - - 14 - - - 30 - - 14 - - 30 - - 30 - - 14 - - 30 - - 30 - - 30 - - 14 - - 30 - - 30 -			$V_{DS} = 5$	00 V, V _{GS}	_s = 0 V	-	-	25	•
orward Transconductance g_{fs} $V_{DS} = 50 \text{ V}, \text{ I}_D = 8.4 \text{ Ab}$ 8.7 $ S$ Dynamic mut Capacitance C_{0ss} $V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1.0 \text{ MHz}, \text{ see fig. 5}$ $ 320$ $ 320$ $ 320$ $ 320$ $ 320$ $ 320$ $ 320$ $ 320$ $ 320$ $ 320$ $ 320$ $ 320$ $ 320$ $ 74$ $ 74$ $ 74$ $ 74$ $ 74$ $ 74$ $ 74$ $ 74$ $ 74$ $ 74$ $ 74$ $ 74$ $ 74$ $ 74$	Zero Gate voltage Drain Current	IDSS	V _{DS} = 400 V, V	/ _{GS} = 0 V	, T _J = 125 °C	-	-	250	μA
DynamicInput CapacitanceCiss $V_{GS} = 0 V$, $V_{DS} = 25 V$, f = 1.0 MHz, see fig. 5-2200-Dutput CapacitanceCoss $V_{GS} = 0 V$, $V_{DS} = 25 V$, f = 1.0 MHz, see fig. 5-2200-Reverse Transfer CapacitanceCrss $\Gamma = 1.0 \text{ MHz}$, see fig. 5-2200-Total Gate ChargeQgQg $V_{GS} = 10 \text{ V}$ Ip = 14 A, $V_{DS} = 400 \text{ V}$, see fig. 6 and 13b74Gate-Drain ChargeQgd $V_{GS} = 10 \text{ V}$ Ip = 14 A, $V_{DS} = 400 \text{ V}$, see fig. 6 and 13b74Sate-Drain ChargeQgd $V_{GS} = 10 \text{ V}$ Ip = 14 A, $V_{DS} = 400 \text{ V}$, see fig. 6 and 13b74Sate-Drain ChargeQgd $V_{GS} = 10 \text{ V}$ Ip = 14 A, $V_{DS} = 400 \text{ V}$, see fig. 6 and 13b74Sate-Drain ChargeQgd $V_{GS} = 10 \text{ V}$ Ip = 14 A, $V_{DS} = 400 \text{ V}$, see fig. 10b14-Turn-Of Delay Timet_d(off) $V_{GS} = 250 \text{ V}$, Ip = 14 A, $R_G = 6.2 \Omega$, $R_D = 17 \Omega$, see fig. 10b-14-Turn-Off Delay Timet_rEBetween lead, form package and center of die contact-5.0-Internal Source InductanceL_SMOSFET symbol showing the integral reverse p - n junction diode14-Palsed Diode Forward CurrentaIsMOSFET symbol showing the integral reverse p - n junction diode14-	Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	ا	_D = 8.4 A ^b	-	-	0.40	Ω
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Forward Transconductance	9 _{fs}	V _{DS} = 5	0 V, I _D =	8.4 A ^b	8.7	-	-	S
Upper Cuput CapacitanceCossVos = 25 V, f = 1.0 MHz, see fig. 5-320-Reverse Transfer CapacitanceCrss $V_{DS} = 25 V,$ f = 1.0 MHz, see fig. 5-320-Total Gate ChargeQgQg $I_D = 14 A, V_{DS} = 400 V,$ see fig. 6 and 13b74Gate-Source ChargeQgd $V_{GS} = 10 V$ $I_D = 14 A, V_{DS} = 400 V,$ see fig. 6 and 13b74Gate-Drain ChargeQgd $V_{GS} = 10 V$ $I_D = 14 A, V_{DS} = 400 V,$ see fig. 6 and 13b14-Turn-On Delay Time $t_{d(on)}$ rurn-Off Delay Time t_{r} $V_{CS} = 10 V$ $I_D = 14 A, V_{DS} = 400 V,$ see fig. 6 and 13b14-Rurn-Off Delay Time $t_{d(off)}$ $V_{CS} = 250 V, I_D = 14 A,$ $R_G = 6.2 \Omega, R_D = 17 \Omega,$ see fig. 10b-14Turn-Off Delay Time $t_{d(off)}$ Between lead, 6 mm (0.25") from package and center of die contact-13Turn-Off Delay Time L_S MOSFET symbol showing the integral reverse $p - n$ junction diode-14Turn-Off Delay Time I_S MOSFET symbol showing the integral reverse $p - n$ junction diode14-Pulsed Diode Forward CurrentaIsMOSFET symbol showing the integral reverse $p - n$ junction diode14-Sody Diode Reverse Recovery Time T_r $T_J = 25 °C, I_F = 14 A, dI/dt = 100 A/µs^b$ -5.07 <td>Dynamic</td> <td></td> <td>•</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	Dynamic		•						
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Input Capacitance	C _{iss}	V			-	2200	-	
Reverse Transfer Capacitance C_{rss} $f = 1.0 \text{ MHz}$, see fig. 5 $ 28$ $-$ Total Gate Charge Q_g Gate-Source Charge Q_{gd} Gate-Drain Charge Q_{gd} Gate-Drain Charge Q_{gd} Turn-On Delay Time $t_{d(on)}$ Rise Time t_r Pun-Off Delay Time $t_{d(off)}$ Rise Time t_r Nurn-Off Delay Time $t_{d(off)}$ Fall Time t_r Nurn-Off Delay Time $t_{d(off)}$ Reg = 6.2 Ω , $R_D = 17 \Omega$, see fig. 10 ^b Fall Time t_r Nurn-Off Delay Time $t_{d(off)}$ Reg = 0.2 Ω , $R_D = 17 \Omega$, see fig. 10 ^b Fall Time t_r Nurn-Off Delay Time $t_{d(off)}$ Total Gate CharacteristicsDrain-Source Body Diode CharacteristicsContinuous Source-Drain Diode Current I_S MOSFET symbol showing the integral reverse $p - n$ junction diodePulsed Diode Forward Currenta I_{SM} Pulsed Diode Reverse Recovery Time t_r $T_J = 25 ^{\circ}$, $I_F = 14 A$, $dI/dt = 100 A/\mu s^b$ $ -$ </td <td>Output Capacitance</td> <td>C_{oss}</td> <td colspan="2">$V_{DS} = 25 V$,</td> <td>-</td> <td>320</td> <td>-</td> <td>pF</td>	Output Capacitance	C _{oss}	$V_{DS} = 25 V$,		-	320	-	pF	
Gate-Source Charge Q_{gs} $V_{GS} = 10 V$ $I_D = 14 \text{ A}, V_{DS} = 400 V,$ see fig. 6 and 13b19nCGate-Drain Charge Q_{gd} Q_{gd} $V_{GS} = 10 V$ $I_D = 14 \text{ A}, V_{DS} = 400 V,$ see fig. 6 and 13b14Gate-Drain Charge Q_{gd} $T_d(on)$ $V_{GS} = 10 V$ $V_{GS} = 10 V$ $V_{SD} = 600 V, I_D = 14 A,$ $V_{DD} = 250 V, I_D = 14 A,$ $R_G = 6.2 \Omega, R_D = 17 \Omega, see fig. 10b-144914141414$	Reverse Transfer Capacitance		f = 1.0	MHz, see	e fig. 5	-	28	-	
Calle-Source ChargeCdgsVGS = 10 Vsee fig. 6 and 13b1316Gate-Drain Charge Q_{gd} Turn-On Delay Time $t_{d(on)}$ Rise Time t_r Turn-Off Delay Time $t_d(off)$ Fall Time t_r Turn-Off Delay Time $t_{d(off)}$ Fall Time t_r Nermal Drain Inductance L_D Between lead, 6 mm (0.25") from package and center of die contactInternal Source Inductance L_S Drain-Source Body Diode CharacteristicsContinuous Source-Drain Diode Current I_S Nusse Provese p - n junction diodePulsed Diode Forward Currenta I_{SM} Body Diode Reverse Recovery Time t_{rr} Rody Diode Reverse Recovery Charge Q_{rr} Turn-Source Recovery Charge Q_{rr}	Total Gate Charge	Qg				-	-	74	
Gate-Drain Charge Q_{gd} $Ion ng r o m r r r d_{d(on)}$ $ 35$ Turn-On Delay Time $t_{d(on)}$ Rise Time t_r Turn-Off Delay Time $t_{d(off)}$ Fall Time t_r $r r r r r r r r r r r r r r r r r r r $	Gate-Source Charge	Q _{gs}	V _{GS} = 10 V			-	-	19	nC
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Gate-Drain Charge			300 1	ilg. 0 and 10	-	-	35	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Turn-On Delay Time	t _{d(on)}				-	14	-	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Rise Time		- 	50 V I	- 14 A	-	49	-	
Internal Drain InductanceLDBetween lead, 6 mm (0.25") from package and center of die contact-5.0Internal Source InductanceLSSetween lead, 	Turn-Off Delay Time	t _{d(off)}	$V_{DD} = 2$ $R_G = 6.2 \Omega, R$	$_{\rm D} = 17 \Omega_{\rm s}$, see fig. 10 ^b	-	30	-	ns
Internal Drain InductanceLD6 mm (0.25") from package and center of die contact-5.0nInternal Source InductanceLS L_S 6 mm (0.25") from package and center of 	Fall Time	t _f				-	30	-	
Internal Source InductanceLSMOSFET symbol showing the integral reverse-13-Drain-Source Body Diode CharacteristicsContinuous Source-Drain Diode CurrentISMOSFET symbol showing the integral reverse14APulsed Diode Forward CurrentaISMISMT_J = 25 °C, IS = 14 A, VGS = 0 Vb1.4VBody Diode Reverse Recovery TimetrrtrrT_J = 25 °C, IF = 14 A, dI/dt = 100 A/µsb-580870nsBody Diode Reverse Recovery ChargeQrrT_J = 25 °C, IF = 14 A, dI/dt = 100 A/µsb-5.17.7µC	Internal Drain Inductance	L _D	6 mm (0.25") fro			-	5.0	-	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Internal Source Inductance	L _S		nter of		-	13	-	nΗ
Continuous Source-Drain Diode CurrentIs Is showing the integral reverse p - n junction diodeshowing the integral reverse p - n junction diode14 14APulsed Diode Forward CurrentaIsmIsmT_J = 25 °C, Is = 14 A, V_Gs = 0 Vb561.4VBody Diode VoltageV_{SDT_J = 25 °C, Is = 14 A, V_Gs = 0 Vb1.4VVBody Diode Reverse Recovery Time t_{rr} T_J = 25 °C, IF = 14 A, dI/dt = 100 A/µsb-580870nsBody Diode Reverse Recovery Charge Q_{rr} 5.17.7µC	Drain-Source Body Diode Characteristic	cs							
Pulsed Diode Forward CurrentaI I SMIntegral reverse p - n junction diode56Body Diode VoltageV SDT T 2 = 25 °C, I S = 14 A, V GS = 0 Vb1.4VBody Diode Reverse Recovery Timet rrt T J = 25 °C, I F = 14 A, dI/dt = 100 A/µsb-580870nsBody Diode Reverse Recovery ChargeQ rrT J = 25 °C, I F = 14 A, dI/dt = 100 A/µsb-5.17.7µC	Continuous Source-Drain Diode Current	۱ _S	showing the	lbol		-	-	14	Δ
Body Diode Reverse Recovery Time t_{rr} $T_J = 25 \text{ °C}, I_F = 14 \text{ A}, dI/dt = 100 \text{ A/}\mu\text{s}^b$ -580870nsBody Diode Reverse Recovery Charge Q_{rr} $T_J = 25 \text{ °C}, I_F = 14 \text{ A}, dI/dt = 100 \text{ A/}\mu\text{s}^b$ -5.17.7 μC	Pulsed Diode Forward Current ^a	I _{SM}	p - n junction die			-	-	56	
$T_{\rm J} = 25 \text{ °C}, I_{\rm F} = 14 \text{ A}, dI/dt = 100 \text{ A}/\mu \text{s}^{\rm b}$ $- 5.1 7.7 \mu \text{C}$	Body Diode Voltage	V _{SD}	T _J = 25 °C, I	_S = 14 A,	$V_{GS} = 0 \ V^{b}$	-	-	1.4	V
Body Diode Reverse Recovery Charge Q _{rr} - 5.1 7.7 μC	Body Diode Reverse Recovery Time	t _{rr}	T ₁ = 25 °C I ₂ -	14 A di/	dt = 100 ۵/۱۱۹ ^b	-	580	870	ns
Forward Turn-On Time ton Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)	Body Diode Reverse Recovery Charge	Q _{rr}	ij - 20 0, if =	, ul/	αι – 100 Αγμο	-	5.1	7.7	μC
	Forward Turn-On Time	t _{on}	Intrinsic turn	on time	is negligible (turn	I-on is doi	minated b	y L _S and	L _D)

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width \leq 300 µs; duty cycle \leq 2 %



Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

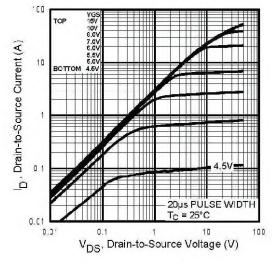


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

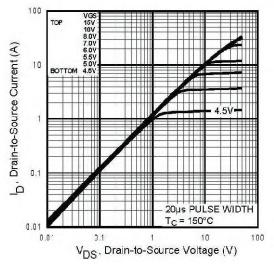


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

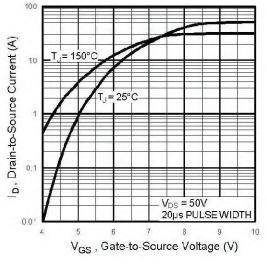


Fig. 3 - Typical Transfer Characteristics

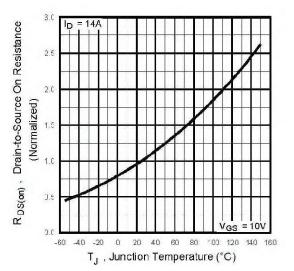


Fig. 4 - Normalized On-Resistance vs. Temperature



Vishay Siliconix

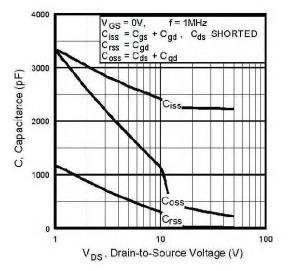


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

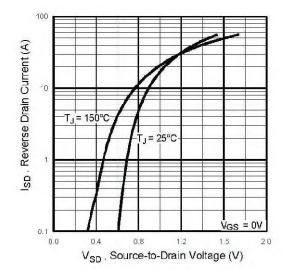


Fig. 7 - Typical Source-Drain Diode Forward Voltage

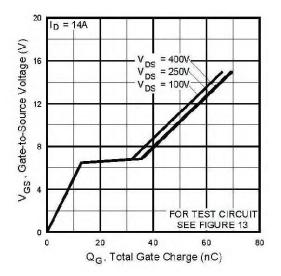


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

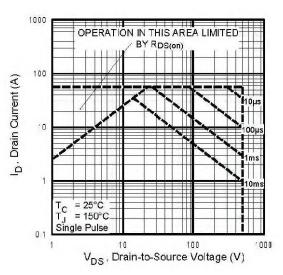


Fig. 8 - Maximum Safe Operating Area



Vishay Siliconix

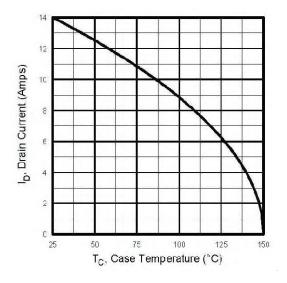


Fig. 9 - Maximum Drain Current vs. Case Temperature

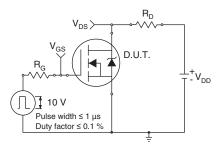


Fig. 10a - Switching Time Test Circuit

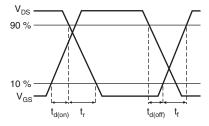


Fig. 10b - Switching Time Waveforms

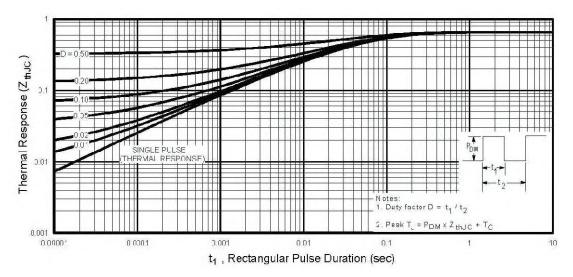


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



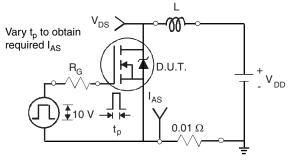


Fig. 12a - Unclamped Inductive Test Circuit

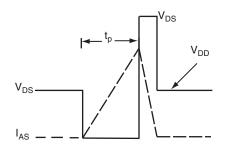


Fig. 12b - Unclamped Inductive Waveforms

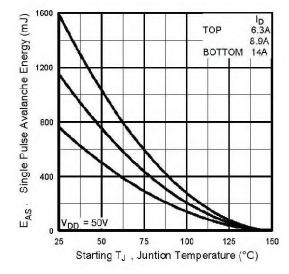
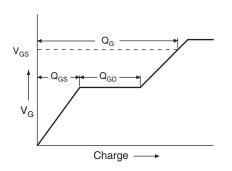
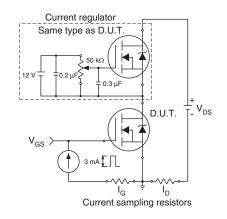


Fig. 12c - Maximum Avalanche Energy vs. Drain Current





S22-0058-Rev. B, 31-Jan-2022





For technical questions, contact: <u>hvmos.techsupport@vishay.com</u> THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT <u>www.vishay.com/doc?91000</u>

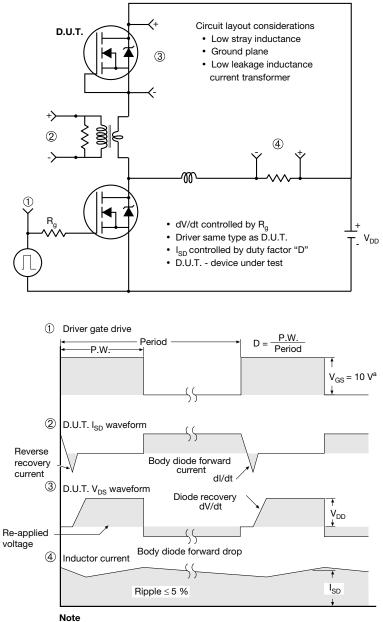
6

IRFP450LC

Vishay Siliconix



Peak Diode Recovery dV/dt Test Circuit



a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91231.





TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9





(

	М	ILLIMETERS		
DIM.	MIN.	NOM.	MAX.	NOTES
А	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
С	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4

		MILLIMETERS	S	
DIM.	MIN.	NOM.	MAX.	NOTES
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
E	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
е		5.46 BSC		
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
ØР	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S		5.51 BSC		

Notes

- ⁽¹⁾ Package reference: JEDEC[®] TO247, variation AC
- (2) All dimensions are in mm
- ⁽³⁾ Slot required, notch may be rounded
- ⁽⁴⁾ Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- ⁽⁵⁾ Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



Vishay Siliconix

VERSION 2: FACILITY CODE = Y



	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
С	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
е	5.46	BSC	
Øk	0.2	254	
L	14.20	16.25	
L1	3.71	4.29	
ØР	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51	BSC	

Notes

- ⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994
- ⁽²⁾ Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- ⁽⁴⁾ Thermal pad contour optional with dimensions D1 and E1
- ⁽⁵⁾ Lead finish uncontrolled in L1
- ⁽⁶⁾ Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- ⁽⁷⁾ Outline conforms to JEDEC outline TO-247 with exception of dimension c

For technical questions, contact: <u>hvm@vishay.com</u> THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT <u>www.vishay.com/doc?91000</u>



Vishay Siliconix

VERSION 3: FACILITY CODE = N



	MILLIMETERS			MILLIMETERS	
DIM.	MIN.	MAX.	DIM.	MIN.	MAX
А	4.65	5.31	D2	0.51	1.35
A1	2.21	2.59	E	15.29	15.87
A2	1.17	1.37	E1	13.46	-
b	0.99	1.40	e	5.46	BSC
b1	0.99	1.35	k	0.:	254
b2	1.65	2.39	L	14.20	16.10
b3	1.65	2.34	L1	3.71	4.29
b4	2.59	3.43	N	7.62	BSC
b5	2.59	3.38	Р	3.56	3.66
С	0.38	0.89	P1	-	7.39
c1	0.38	0.84	Q	5.31	5.69
D	19.71	20.70	R	4.52	5.49
D1	13.08	-	S	5.51	BSC

Notes

⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994

⁽²⁾ Contour of slot optional

(3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body

⁽⁴⁾ Thermal pad contour optional with dimensions D1 and E1

⁽⁵⁾ Lead finish uncontrolled in L1

⁽⁶⁾ Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



Vishay

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

© 2024 VISHAY INTERTECHNOLOGY, INC. ALL RIGHTS RESERVED

Revision: 01-Jan-2024